In the Specification:

Please replace the paragraph beginning at page 1, line 19 with the following rewritten paragraph:

Fig. 1 is a block diagram 10 illustrating the use of virtual memory management of the prior art. The CPU has a plurality of virtual memory addresses 20 used by the operating system and/or application software 23. The virtual address 20 is translated into a physical address 30 through a page table look-up 25. The physical address 30 drives memory decode logic 35 to access the appropriate memory resources 40a-40d. The memory decode logic (e.g. motherboard chipset), while possibly configurable at boot ~~tome~~ time (e.g. by BIOS), is static in that it does not change at runtime. For example, for a given address, the memory decode logic always selects the same memory device. Accordingly, the page look-up table 25 translates the virtual address of the CPU to a physical memory address under the direction of the operating system 27.

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